REMARKS

Claim 1 has been amended. New claims 5 and 6 have been added. Claim 5 discloses features somewhat similar to amended claim 1. Claim 6 includes the allowable subject matter of "objected to" claim 3.

Claims 1-6 are currently pending and under consideration. Reconsideration is respectfully requested.

I.   **REJECTION OF CLAIMS 1-4 UNDER 35 U.S.C. 103(a) AS BEING UNPATENTABLE OVER TAWARA ET AL. (U.S. PATENT NO. 4,926,415) IN VIEW OF KOSONOCKY ET AL. (U.S. PATENT NO. 5,361,343):**

None of the foregoing references, individually or combined, discloses "a method of managing a memory device, said memory device comprising a memory area comprising at least one flash memory and a controller for controlling data writing to the memory area, the method comprising: sending from a host computer to the controller a size of data to be written from the host computer to the memory area; and causing the controller to estimate a length of time to be required for writing the data into the memory area on a basis of the size of the data and conditions of the memory area, said conditions indicating at least whether data evacuation is necessary, " as recited in amended claim 1, for example.

In contrast, Tawara discloses a network interface in a LAN system for transferring a message from a first terminal to a second terminal at high speed. That is, Tawara is directed to message transmission over a network (see Abstract). Tawara further discloses a CPU 14 of a network interface unit 4 including a size detection section for detecting the size of the message sent from terminal 2 and a detection section for detecting a packet size of a packet to be transmitted to another network interface unit (see FIG. 4 and column 4, lines 33-44).

At page 3 The Examiner admits that Tawara fails to disclose estimating a length of time to be required for writing the data into the memory area based on the size/condition of the data. However, the Examiner asserts that Kosonocky discloses this feature.

The Applicants respectfully submit that neither Tawara nor Kosonocky, individually or combined, disclose "causing the controller to estimate a length of time to be required for writing the data into the memory area on a basis of the size of the data and conditions of the memory area, said conditions indicating at least whether data evacuation is necessary, " as recited in amended claim 1, for example.

Instead, Kosonocky merely discloses a microprocessor system including a first and a second nonvolatile memory array which may be simultaneously read and reprogrammed (see column 2, lines 50-54). Specifically, Kosonocky discloses that time required for programming is dependent on the size of the memory array of a flash memory (see column 2, lines 5-6). That is, Kosonocky does not disclose a controller **actually** "estimating a length of time to be required for writing the data into the memory area," as recited in claim 1, for example. Nor does Kosonocky disclose "estimate a length of time … on a basis of the size of the data and conditions of the memory area, said conditions indicating at least whether data evacuation is necessary," as recited in amended claim 1, for example.

Therefore, the combination of Tawara and Kosonocky fails to establish a prima facie case of obviousness over the present invention.

Thus, withdrawal of the rejections is respectfully requested.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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